



SY73551L

160MHz 1:4 LVCMOS/LVTTL
Fanout Buffer

General Description

The SY73551L is a high speed 1:4 LVCMOS/LVTTL fanout buffer. Its LVCMOS/LVTTL logic-compatible input is reproduced four times by LVCMOS/LVTTL outputs with less than 250ps of skew and only 63fs_{RMS} of additive phase jitter.

The non-inverting outputs have low impedance and are capable of driving 50Ω transmission lines. An output enable function provides the ability to tri-state the output signals.

The SY73551L operates from a 3.3V ±10% power supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. It is available in an 8-pin SOIC package. The SY73551L is part of Micrel's Precision Edge[®] product line.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

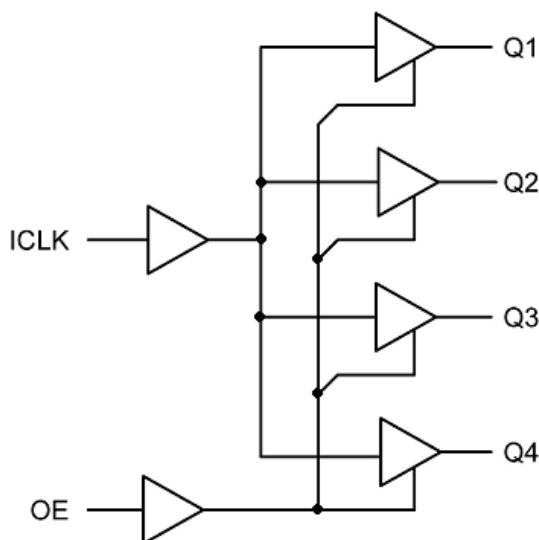
Features

- Accepts LVCMOS and LVTTL input signal levels
- Outputs LVCMOS and LVTTL signal levels
- 160MHz maximum operating frequency
- Low skew outputs: 250ps max. skew
- Ultra-low jitter: 63fs_{RMS}
- Non-inverting output clock
- Output enable feature tri-states outputs
- 3.3V ±10% power supply
- Industrial temperature range: -40°C to +85°C
- Available in Pb-free 8-pin SOIC package

Applications

- Clock distribution
- High performance PCs
- Communications systems
- Parallel processor-based systems

Functional Block Diagram



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September 19, 2013

Revision 1.0 (final document)
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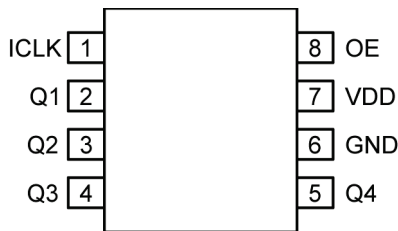
Ordering Information

Part Number ⁽¹⁾	Package Type	Operating Range	Package Marking	Lead Finish
SY73551LZG	Z8-1	Industrial	73551L with Pb-free bar-line indicator	NiPdAu
SY73551LZGTR ⁽²⁾	Z8-1	Industrial	73551L with Pb-free bar-line indicator	NiPdAu

Note:

- Contact factory for die availability. Die is guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
- Tape and Reel.

Pin Configuration



8-Pin SOIC

Pin Description

Pin Number	Pin Name	Pin Function
1	ICLK	Single-ended clock input. Accepts LVCMOS and LVTTTL input levels. Connected to internal pull-up resistor. See Pin Characteristics table for typical values.
2	Q1	Outputs. Non-inverted single-ended buffered copies of the input signal. 3.3V LVCMOS- and LVTTTL-compatible outputs.
3	Q2	
4	Q3	
5	Q4	
6	GND	Power supply pin. Connect to ground.
7	VDD	3.3 V $\pm 10\%$ power supply: Bypass with 0.1 μF /0.01 μF low ESR capacitors as close to the V _{DD} pin as possible.
8	OE	Output enable input: Single-ended input. Accepts LVTTTL input levels. Tri-states outputs when low. Connected to internal pull-up resistor. See Pin Characteristics for typical values.

Absolute Maximum Ratings⁽³⁾

Supply Voltage (V_{DD}).....	+4.0V
Input Voltage (V_{IN}).....	-0.5V to V_{DD} +0.5V
Output Voltage (V_O).....	-0.5V to V_{DD} +0.5V
Lead Temperature (soldering, 20s).....	260°C
Maximum Junction Temperature.....	125°C
Storage Temperature (T_s).....	-65°C to +150°C

Operating Ratings⁽⁴⁾

Supply Voltage (V_{DD}).....	+3.0V to +3.6V
Ambient Temperature (T_A).....	-40°C to +85°C
Junction Thermal Resistance	
SOIC (θ_{JA}), Still-Air	93°C/W

Pin Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	ICLK, OE pins		5		pF
R_{PUP}	Input pull-up resistor	ICLK, OE pins		250		k Ω
Z_{OUT}	Output impedance	Q0-Q3 pins		10		Ω

DC Electrical Characteristics⁽⁵⁾

V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Power supply voltage	Operational voltage range	3.0	3.3	3.6	V
I_{DD}	Power supply current	No load, 135MHz		18		mA

ICLK Pin Electrical Characteristics⁽⁵⁾

V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	Nominal switching threshold is $V_{DD}/2$	$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	Input low voltage	Nominal switching threshold is $V_{DD}/2$	0		$V_{DD}/2 - 0.7$	V

OE Pin Electrical Characteristics⁽⁵⁾

V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	Nominal switching threshold is 1.4V	2.0		V_{DD}	V
V_{IL}	Input low current	Nominal switching threshold is 1.4V	0		0.8	V

Output DC Electrical Characteristics⁽⁵⁾

$V_{DD} = 3.0V$ to $3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage (CMOS)	$I_{OH} = -12mA$	$V_{DD} - 0.4$			V
V_{OH}	Output high voltage	$I_{OH} = -25mA$	2.4			V
V_{OL}	Output low voltage	$I_{OL} = 25mA$			0.4	V

Notes:

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Specification for packaged product only

AC Electrical Characteristics^(6, 8)

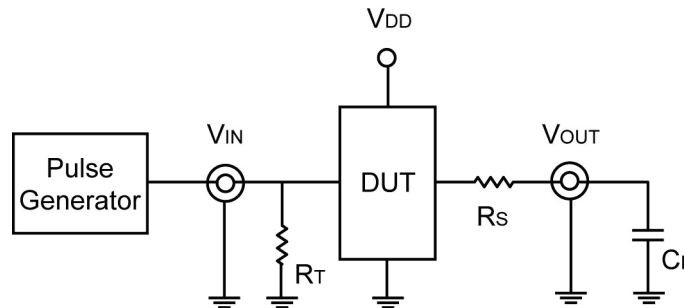
$V_{DD} = 3.0V$ to $3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{MAX}	Maximum frequency		160	200		MHz
$T_{PD}^{(7)}$	Propagation delay	$ICLK \rightarrow Q_N$, $F = 135MHz$	2	4	8	ns
t_r/t_f	Output rise time	0.8V to 2.0V, Note 8			1	ns
	Output fall time	2.0V to 0.8V, Note 8			1	ns
T_{SKEW}	Output-to-output skew	Note 9		100	250	ps
Duty Cycle	Output duty cycle	50/50% input duty cycle	45	50	55	%
T_{JIT}	Additive phase jitter	At 156MHz, 12k to 20M integration range		63		fs _{RMS}

Notes:

- The circuit is designed to meet the AC specifications shown in the table above after thermal equilibrium has been established.
- Measured with rail-to-rail input.
- Refer to Page 5 for test circuit, $R_S = 33\Omega$ and $C_L = 15pF$.
- Output-to-output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, transition, and loading.

AC Output Test Circuit



Test Conditions

Symbol	Condition	Units
R_T	Z_{OUT} of pulse generator	Ω
t_r/t_f Generator	1 (0V to V_{DD})	ns
	1 (V_{DD} to 0V)	ns
R_S	33	Ω
C_L	15	pF

Definitions:

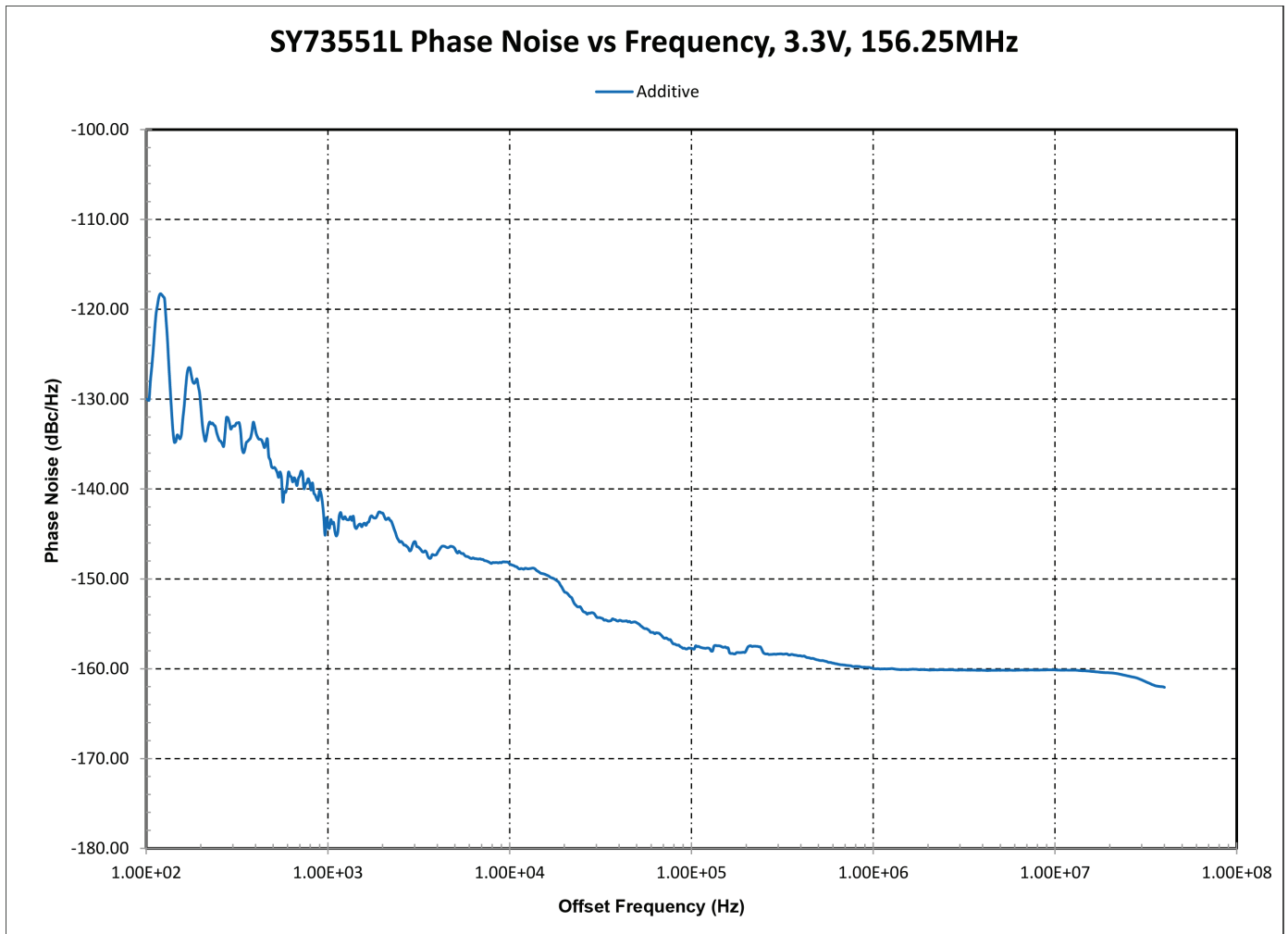
R_T = Termination resistance, typically equal to the Z_{OUT} of the pulse generator.

t_r/t_f = Rise and fall times of the input from the pulse generator at the DUT input pin.

R_S = Dynamic matching resistor

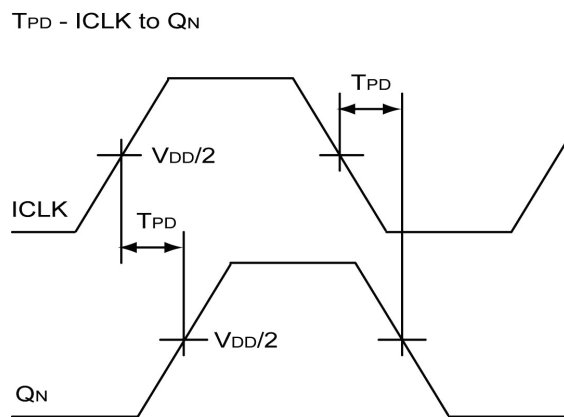
C_L = Load capacitance, including fixture and probe capacitance.

Phase Noise Plots

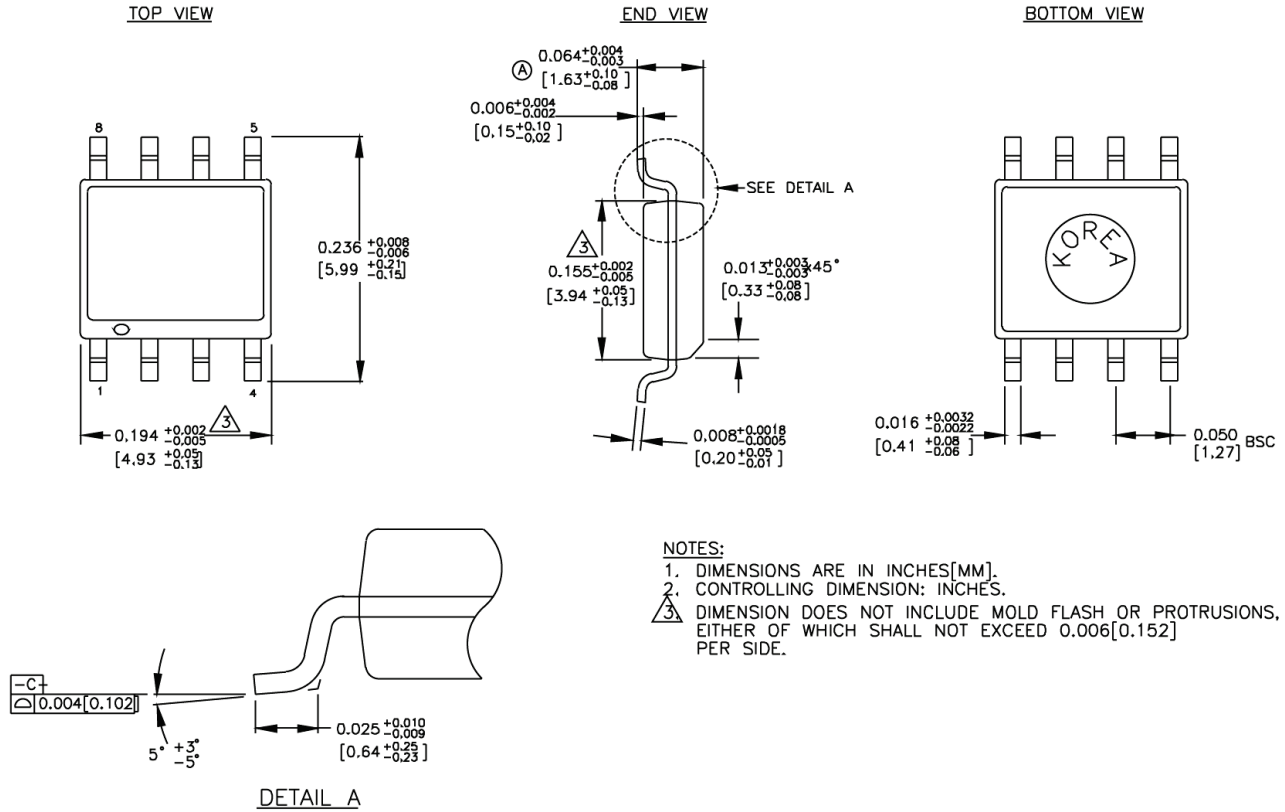


SY73551L Phase Noise vs. Frequency

AC Switching Waveform



Package Information⁽¹⁰⁾



Rev.03

8-Pin SOIC

Note:

10. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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